

Panasonic Liquid Crystal Display Co.,Ltd.

Sep.13,2012

TECHNICAL DATA

⁹⁰
VVX10F002A00

CONTENTS

No.	Item	Page
-	COVER	1-1/1
-	RECORD OF REVISION	2-1/2~2/2
-	DESCRIPTION	3-1/1
1	ABSOLUTE MAXIMUM RATINGS	4-1/2~2/2
2	INITIAL OPTICAL CHARACTERISTICS	5-1/3~3/3
3	ELECTRICAL CHARACTERISTICS	6-1/1
4	BLOCK DIAGRAM	7-1/1
5	INTERFACE PIN ASSIGNMENT	8-1/3~3/3
6	INTERFACE TIMING	9-1/7~7/7
7	DIMENSIONAL OUTLINE	10-1/3~3/3
8	LABEL FORMAT	11-1/1
9	COSMETIC SPECIFICATIONS	12-1/2~2/2
10	PACKING	13-1/2~2/2

DESCRIPTION

The following specifications are applied to the following TFT LCD module.

Product Name : ~~VVX10F002A00~~⁰⁰

General Specifications

Effective display area	: (H) 217.44 × (V) 135.90	(mm)
Number of pixels	: (H) 1,920 × (V) 1,200	(pixels)
Pixel pitch	: (H) 0.11325 × (V) 0.11325	(mm)
Color pixel arrangement	: R+G+B	vertical stripe
Display mode	: Transmissive mode Normally black mode	
Top polarizer type	: Low Reflection Coat + Retardation Film	
Number of colors	:16,777,216	(colors)
Input signal	: MIP1 4 Lanes	
Backlight	: 36 pieces of LED	
External dimensions	: Typ. (H) 228.96 × (V) 148.5 × (t) 2.299 (PCB side 4.13 (mm)	
Weight	: 136g max.	

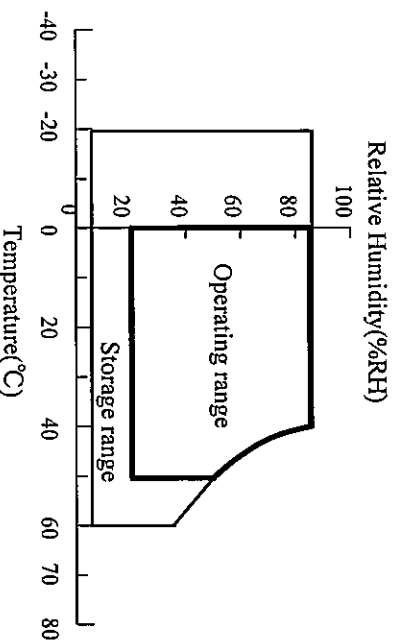
1. ABSOLUTE MAXIMUM RATINGS

1.1 Environmental Absolute Maximum Ratings

ITEM	Operating		Storage		UNIT	NOTE
	Min.	Max.	Min.	Max.		
Temperature	0	50	-20	60	°C	1),3)
Humidity	2)				%RH	1)
Vibration	-	-	4)		m/s ²	
Shock	-	-	5)		m/s ²	
Corrosive Gas	Not Acceptable		Not Acceptable		-	
Illumination at LCD Surface	-	50,000	-	50,000	lx	

Note 1) Temperature and Humidity should be applied to the glass surface of a IPS-Pro TFT LCD module, not to the system installed with a module.

- 2) $T_a \leq 40^\circ\text{C}$ Relative humidity should be less than 85 %RH max. Dew is prohibited.
 $T_a > 40^\circ\text{C}$ Relative humidity should be lower than the moisture of the 85 %RH at 40°C .



- 3) The temperature of LCD front surface would be 65°C in operating, it may affect the optical characteristics however it does not damage the function of the module.
- 4) Sine vibration(Non-operation) 3.5G Zero to peak, 30min One sweep 10 to 500Hz, all 3 axes(X,Y,Z).
- 5) Shock(Non-operation) Half sine 30.6G, duration time 18ms. Velocity change : 3.4m/s

1. 2 Electrical Absolute Maximum Ratings

(1) TFT-LCD module

V_{SS} = 0 V

ITEM	SYMBOL	Min.	Max.	UNIT	NOTE
Power Supply Voltage	VBAT	0	5.0	V	
Input Voltage for LED driver	VDD+	-0.3	5.0	V	
Input Voltage for logic	VI	-0.3	2.8	V	1)
Electrostatic Durability	VESD0	+ / - 6.		kV	2)
	VESD1	+ / - 8		kV	3)

Note 1) It is applied to IOVDD, SCL, SDA, LED_EN, LEDPWM.

2) Non-operation , Contact discharge , 150 pF / 330 ohms.

3) Non-operation , Air discharge , 150 pF / 330 ohms.

Panasonic Liquid Crystal Display Co., Ltd.	Date	Sep.13,2012	No.	ATD5231-6	Page	4-2/2
--	------	-------------	-----	-----------	------	-------

2. INITIAL OPTICAL CHARACTERISTICS

The following optical characteristics are measured under stable conditions. It takes about 30 minutes to reach stable conditions. The measuring point is the center of display area unless otherwise noted.

The optical characteristics should be measured in a dark room or equivalent state.

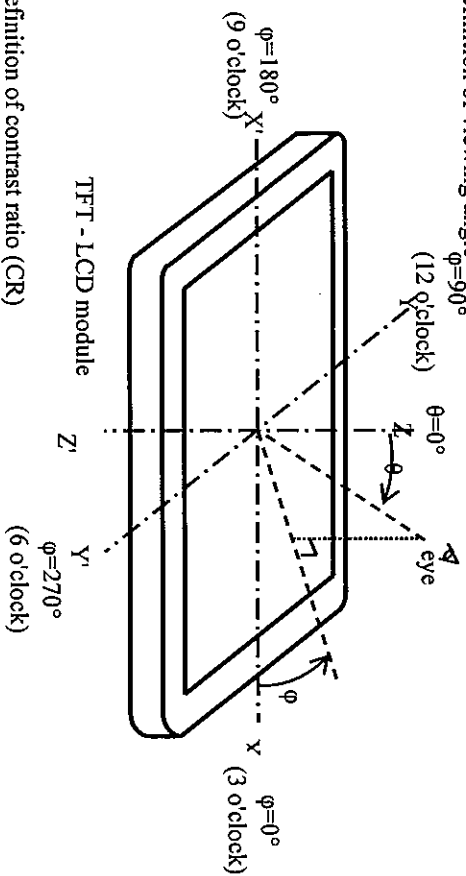
Measuring equipment : CS-1000A, or equivalent

Ambient Temperature =25 °C, AV_{DD}=3.1 ~4.2V, f_v=60 Hz,

IF=20mA (on duty 100%)

ITEM	SYMBOL	CONDITION	Min.	Typ.	Max.	UNIT	NOTE
Contrast ratio	CR	$\theta = 0^\circ$ 1)	600	1000	-	-	1),2)
Response time (Rise + Fall)	Tr + Tf	$\theta = 0^\circ$ 1)	-	-	30	ms	1),3)
Brightness of white	B _{wh}		360	450	-	cd/m ²	1)
Brightness uniformity	B _{unif} (points)		70	80	-	%	1),4)
Color chromaticity (CIE)	Red		0.580	0.610	0.640	-	1) 【Gray scale =255】
			0.310	0.340	0.370		
	Green		0.290	0.320	0.350		
			0.510	0.540	0.570		
	Blue		0.120	0.150	0.180		
			0.080	0.110	0.140		
	White		0.275	0.310	0.345		
			0.285	0.320	0.355		
			100	-	-		
View Angle	Right	$\theta=80^\circ, \phi=0^\circ$	100	-	-	-	1)
	Left	$\theta=80^\circ, \phi=180^\circ$	100	-	-		
	Top	$\theta=80^\circ, \phi=90^\circ$	100	-	-		
	Bottom	$\theta=80^\circ, \phi=270^\circ$	100	-	-		
NTSC	-	$\theta = 0^\circ$ 1)	40	50	-	%	1)
W,R,G,B Gamma	-	$\theta = 0^\circ$	2.2	2.5	2.8	-	1)
Cross talk	-	$\theta = 0^\circ$	-	-	3	%	5)

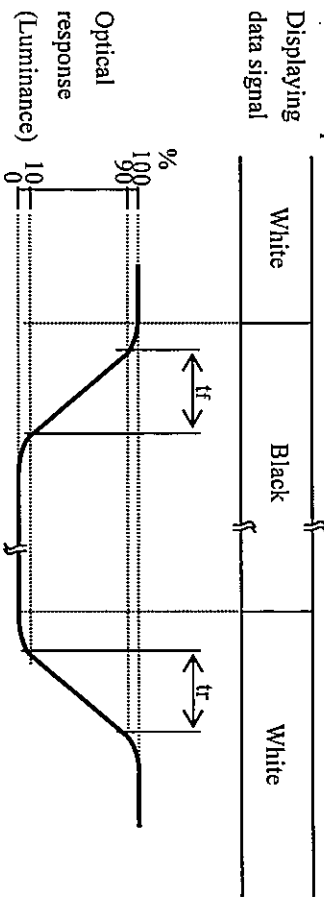
Note 1) Definition of viewing angle $\phi=90^\circ$



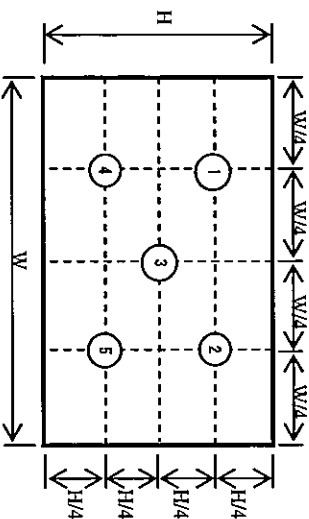
2) Definition of contrast ratio (CR)

$$CR = \frac{\text{Luminance at displaying WHITE}}{\text{Luminance at displaying BLACK}}$$

3) Definition of response time



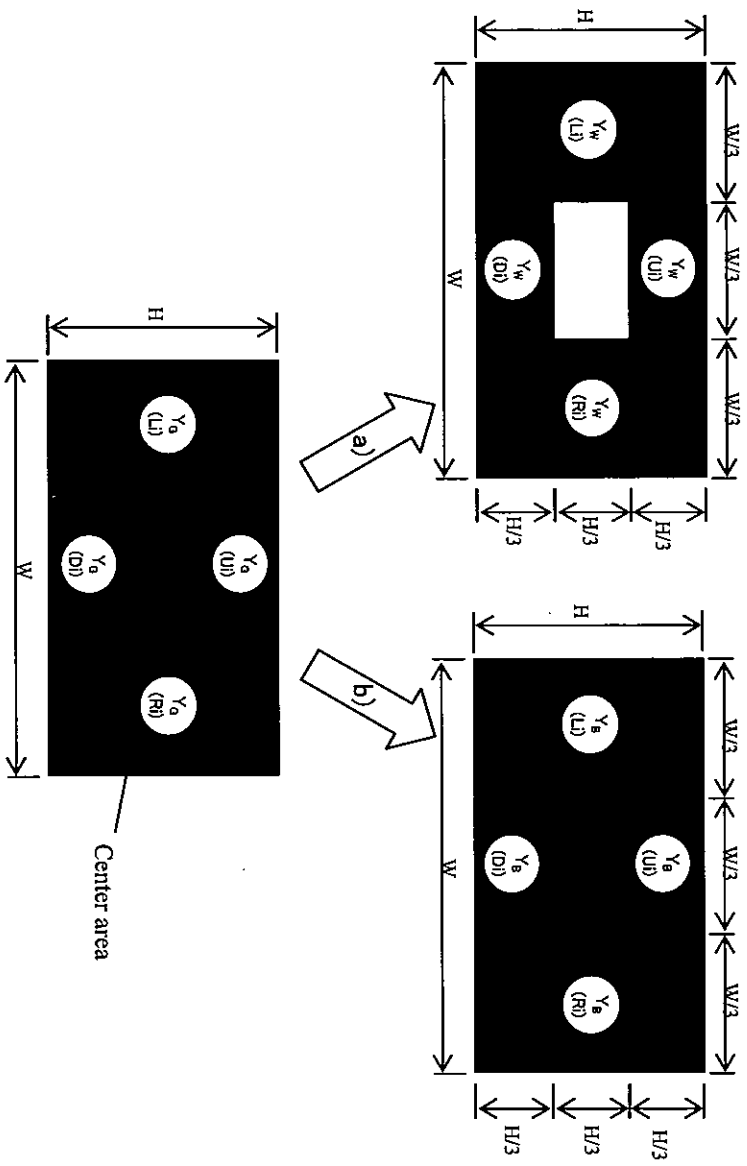
4) Definition of Uniformity



①~⑤ measuring points

$$\text{Buri (5 Points)} = \min(\text{①} \sim \text{⑤}) / \max(\text{①} \sim \text{⑤})$$

Note 5) Definition of Cross talk



a) Center area : White

$$CT = \frac{|Y_w(X_{127}) - Y_g(X_{127})|}{Y_g(X_{127})} \times 100\%$$

b) Center area : Black

$$CT = \frac{|Y_b(X_{127}) - Y_g(X_{127})|}{Y_g(X_{127})} \times 100\%$$

Note: $x=U,D,L$ and R, X_{127} = Gray scale 127

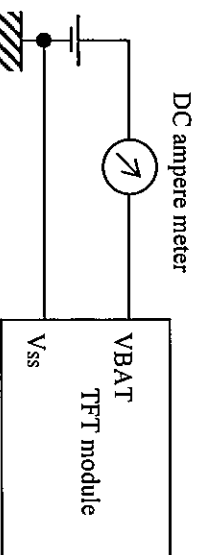
3. ELECTRICAL CHARACTERISTICS

3.1 TFT-LCD module

Ta = 25 °C, Vss = 0 V

ITEM	SYMBOL	Min.	Typ.	Max.	UNIT	NOTE
Power supply voltage	VBAT	3.1	3.7	4.2	V	
Power supply current	I _{DD}	-	(0.4)	(0.6)	A	1)
Ripple voltage of power supply	V _{DDR}	-	-	(100)	mV	
Input voltage for LED driver	VDD+	3.1	3.7	4.2	V	
Input voltage for logic	V _I	1.7	1.8	1.9	V	
Logic signals input voltage	High	V _{IH}	(V _I *0.65)	-	V	LED_EN,
	Low	V _{IL}	-	(V _I *0.3)	V	LEDPWM
I2C BUS input voltage	High	V _{IH2}	1.7	-	V	SCL, SDA
	Low	V _{IL2}	-	0.4	V	
Logic signal output voltage	High	V _{OH}	(V _I -0.2)	-	V	VSYNC, HSYNC
	Low	V _{OL}	-	(0.2)	V	

Note 1)



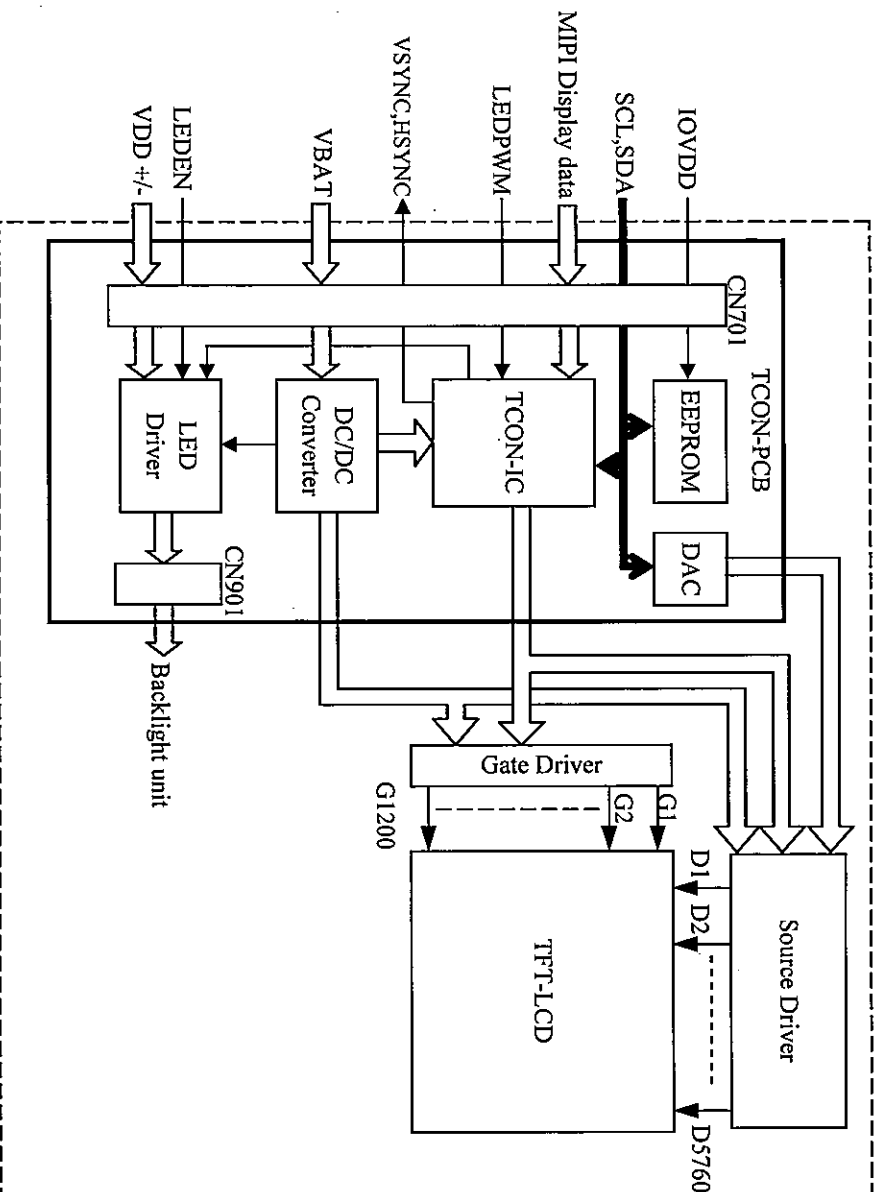
3.2 Backlight unit

ITEM	SYMBOL	Min.	Typ.	Max.	UNIT	NOTE
Power Consumption	P _{bl}	-	2.1	2.4	W	(1), 2)
	Duty	0	-	100	%	
PWM	Frequency	PF	100	-	20k	Hz

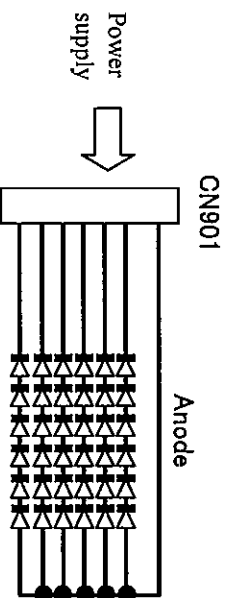
- Note 1) This characteristics should be applied putting on the LED about 60 minutes later with ambient temperature.
(Ta = 25 °C ± 2 °C)
- 2) This value is not include LED driver loss.

4. BLOCK DIAGRAM

4.1 TFT-LCD module



4.2 Backlight unit



5. INTERFACE PIN ASSIGNMENT

5.1 TFT-LCD module

CN701:1-I-PEX (20474-040E-12)

PIN No.	SYMBOL	DESCRIPTION	Note
1	VBAT	Power supply for analog	1)
2	VBAT		
3	VBAT		
4	IOVDD	Power supply for I/O	
5	VSYNC	VSYNC output from Tcon	
6	GND	GND(0V)	2)
7	GND		
8	HSYNC	HSYNC output from Tcon	
9	LEDPWM	PWM input	
10	SDA	I2C-bus Data	
11	SCL	I2C-bus Clock	
12	LED_EN	LED enable	
13	CTS0/ID0	Pull down 510kohm to GND	
14	CTS1/ID1	Pull down 510kohm to GND	
15	GND	GND(0V)	2)
16	DSI_D2P/Rx-IN2P	MIPi data pair 2 positive signal	
17	DSI_D2N/Rx-IN2P	MIPi data pair 2 negative signal	
18	GND	GND(0V)	2)
19	DSI_D1P/Rx-IN1P	MIPi data pair 1 positive signal	
20	DSI_D1N/Rx-IN1N	MIPi data pair 1 negative signal	

PIN No.	SYMBOL	DESCRIPTION	Note
21	GND	GND(0V)	2)
22	DSI_CLKP/Rx-CLKP	MIPi Clock positive signal	
23	DSI_CLKN/Rx-CLKN	MIPi Clock negative signal	
24	GND	GND(0V)	2)
25	DSI_D0P/Rx-IN0P	MIPi data pair 0 positive signal	
26	DSI_D0N/Rx-IN0N	MIPi data pair 0 negative signal	
27	GND	GND(0V)	2)
28	DSI_D3P/Rx-IN3P	MIPi data pair 3 positive signal	
29	DSI_D3N/Rx-IN3N	MIPi data pair 3 negative signal	
30	GND	GND(0V)	2)
31	BIST	Keep open or connect to GND	4)
32	VDD-	GND(0V)	
33	VDD-		
34	VDD-		
35	VDD-	No connection	
36	NC		
37	VDD+		
38	VDD+	Power supply for VDD	3)
39	VDD+		
40	VDD+		

Notes 1) All VBAT pins shall be connected to +3.1~4.2V.

2) All GND pins shall be grounded. Metal bezel is internally connected to GND.

3) All VDD+ pins shall be connected to +3.1~4.2V.

4) Note. pin. 31

Our T-CON (NT71391) has CABC function, but it cannot t

CABC can be controlled by the configuration data (disenab

Please keep pin.31 open setting.

5) Please do not use the following address.

A0(hex),E8 (hex)

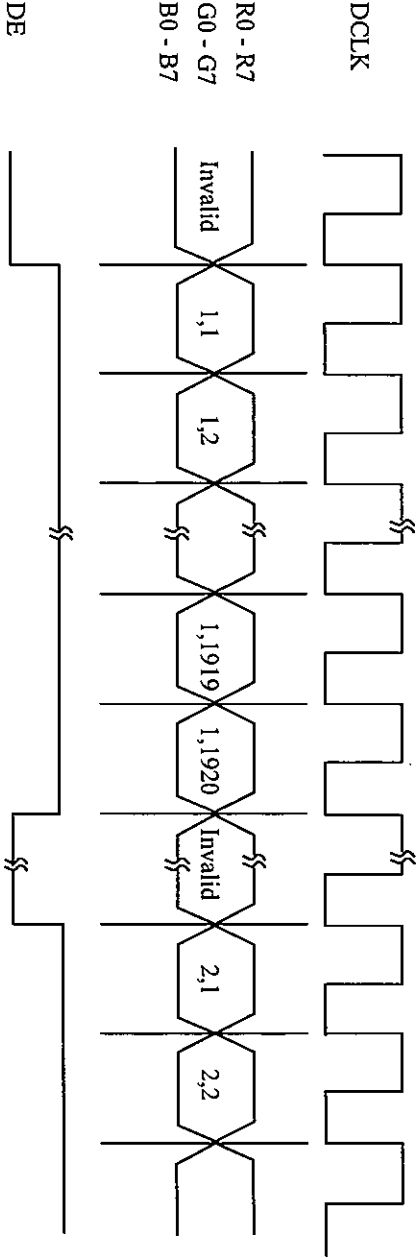
5.2 Correspondence between input data and display image

Display data of adjacent two pixel is latched during four cycle of CLK.

R	G	B
(1,1)	(1,1)	(1,1)

Pixel : R0 - R7 : R (x,y)
G0 - G7 : G (x,y)
B0 - B7 : B (x,y)

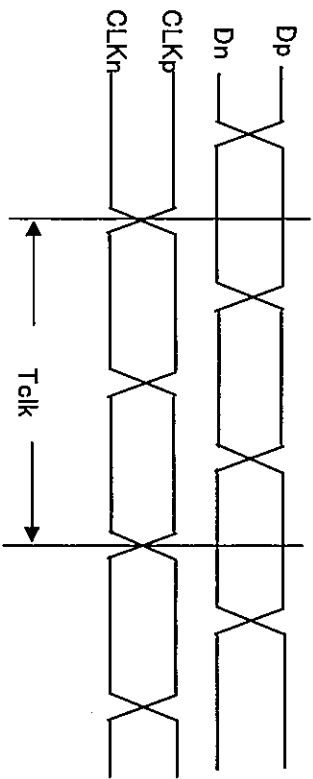
1, 1	1, 2	1, 3	-----	1, 1920
2, 1	2, 2	2, 3	-----	2, 1920
3, 1	3, 2	3, 3	-----	3, 1920
-----	-----	-----	-----	-----
-----	-----	-----	-----	-----
-----	-----	-----	-----	-----
-----	-----	-----	-----	-----
1200, 1	1200, 2	1200, 3	-----	1200, 1920



6. INTERFACE TIMING

6.1 MPI receiver timing

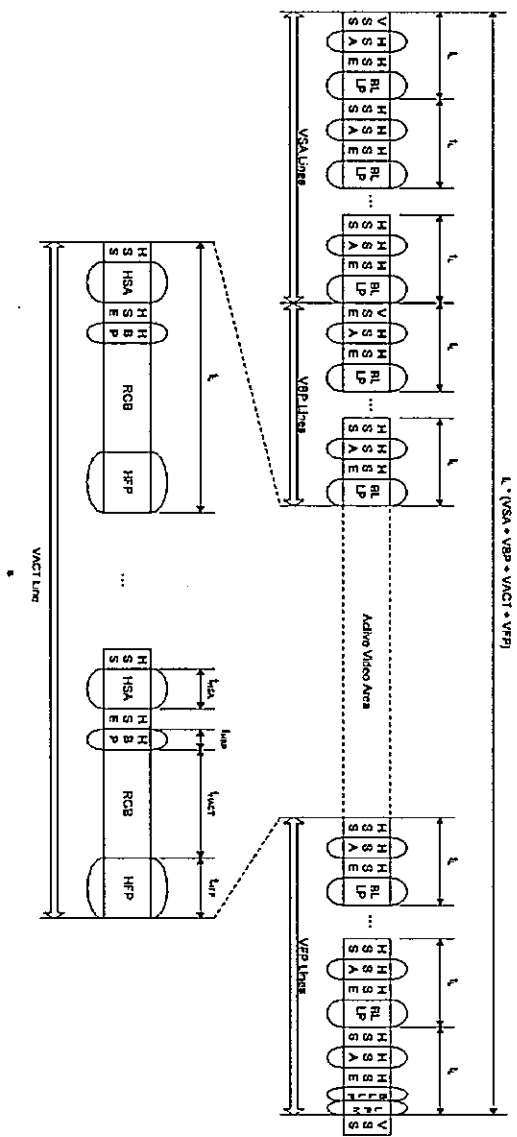
(1) High Speed CLK Timing



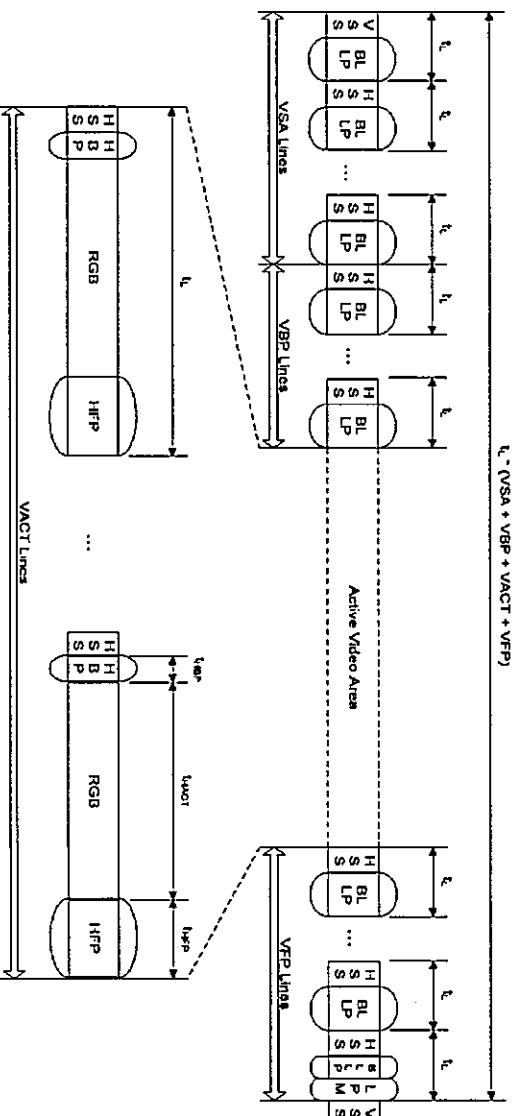
	Min	Max
Tclk	2ns(500MHz)	10ns(100MHz)

(2) Data Transmission Timing

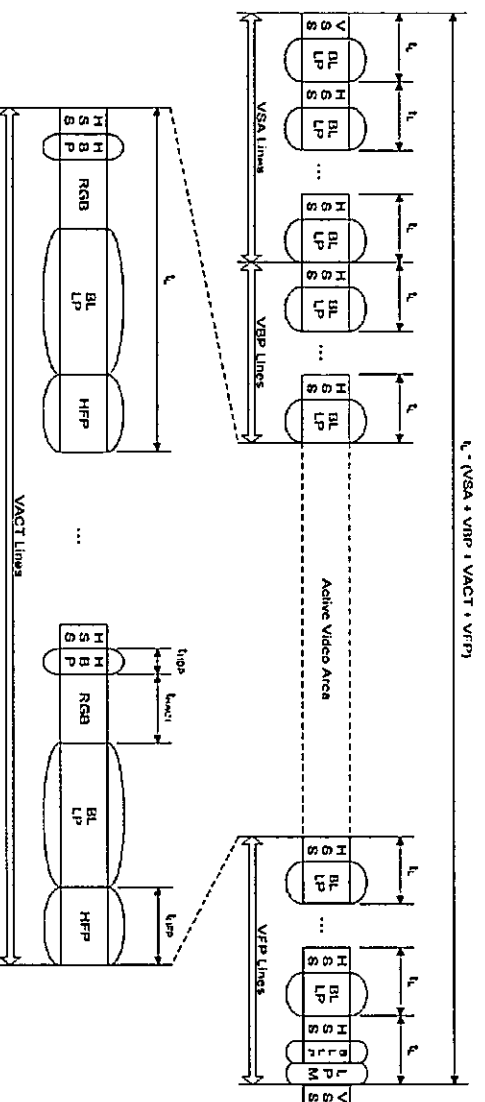
(i) Non-Burst Transmission with Sync Start and End (Pulse Mode)



(ii) Non-Burst Transmission with Sync Events (Event Mode)



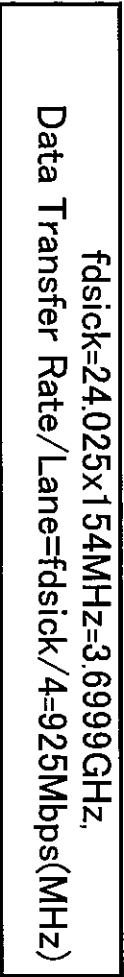
(iii) Burst Mode



(iv) Supplemental Information

- (1) HFP in any above three modes can be replaced with L-P-11 state (idle mode). Length of L-P-11 state and transition period from L-P-11 state to HS ($T_{HSSETTLE}$) and the period from HS to L-P-11 ($T_{HS-TRAIL} + T_{HS-EXIT}$) shall meet the specification of the timing specified in the D-PHY standard of the MIPI interface.
- (2) Data can be transferred in any mode of above three without telling the panel which mode is used.
- (3) No EoT packet(not EoT protocol) is required.
- (4) The line frequency (fH) and frame frequency (fV) of the timing in any above three modes shall fall in the range between Min and Max value specified in the table in the section 6.2.

fdot=2080x1235x60=154MHz
Tdot=1/154MHz=6.49ns
fh=1235x60=74.1kHz
TH=13.495us



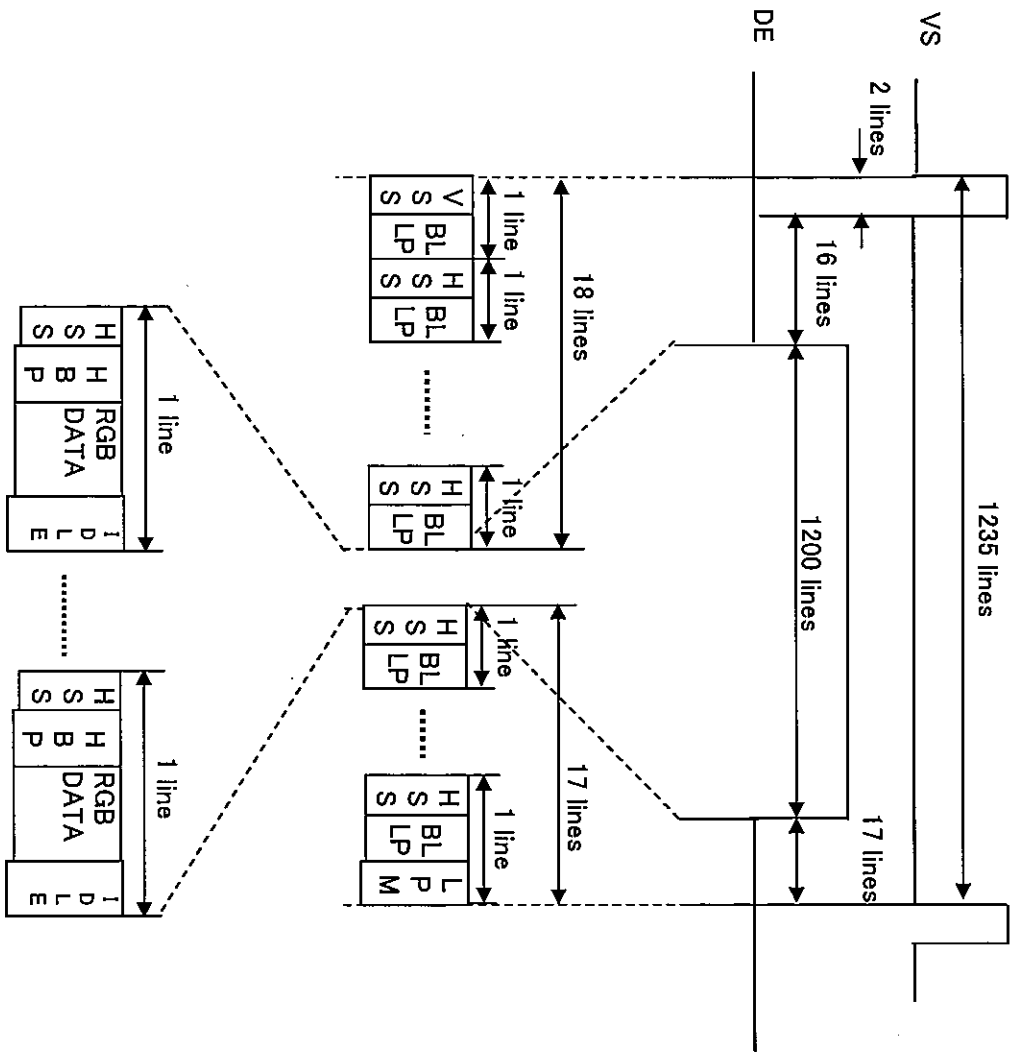
Panasonic Liquid Crystal Display Co., Ltd.

Sep.13,2012

ATD5231-6

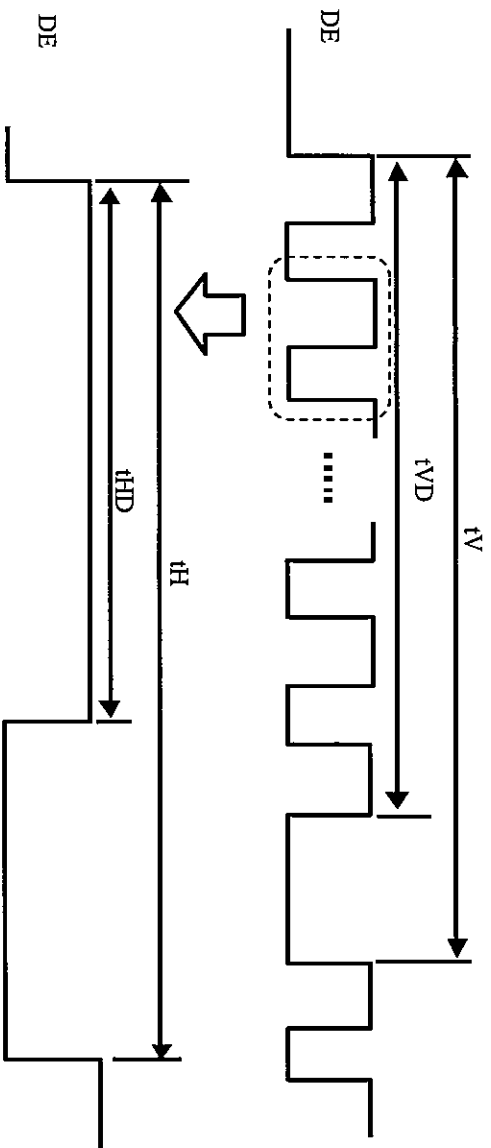
9-317

(vi) An Example of Non-Burst Event Mode DSI Timing (Frame Period)



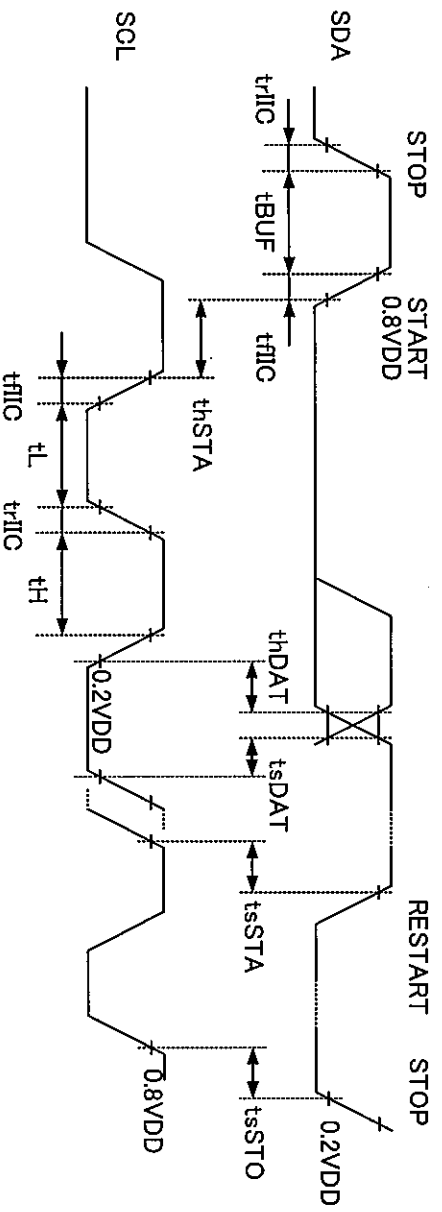
1 Line =50.052 DStick
TH=50.052/3.6999GHZ=13.5us
TV=1235xTH
=1235x50.052/3.6999GHZ
=16.7ms
FV=1/TV=60Hz

6.2 SYNCHRONIZATION SIGNAL TIMING



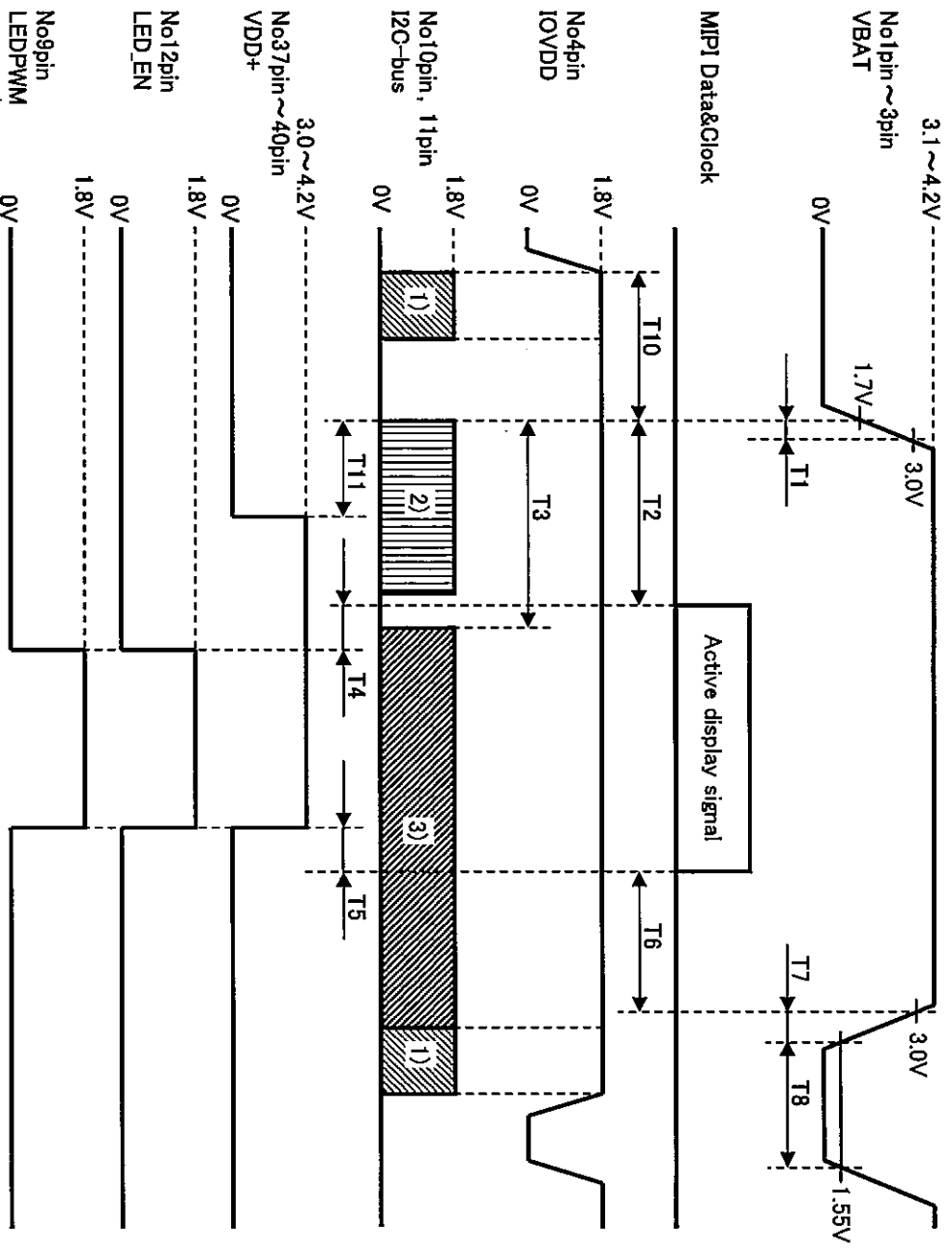
ITEM	SYMBOL	Min.	Typ.	Max.	UNIT	NOTE
Vertical Frequency	f_V	58	60	62	Hz	
Vertical Period	t_V	1216	1235	1253	t_H	
Vertical Valid	t_{VD}		1200		t_H	
Horizontal Frequency	f_H	73	74	75	KHz	
Horizontal Period	t_H	2042	2080	2120	t_{CLK}	
Horizontal Valid	t_{HD}		1920		t_{CLK}	

6.3 I2C timing



Parameter	Symbol	Conditions	Rating			Unit
			MIN	TYP	MAX	
SCL Clock Frequency	fsc1		1	-	100	kHz
STOP START Interval	tBUF		4.7	-	-	μs
START HOLD Time	thSTA		4.0	-	-	μs
RESTART SETUP Time	tsSTA		4.7	-	-	μs
STOP SETUP Time	tsSTO		4.7	-	-	μs
Rize Time	tR1C	See. Upper Fig.	-	-	1.0	μs
Fall Time	tF1C		-	-	0.3	μs
Clock Low Time	tL		4.7	-	-	μs
Clock High Time	tH		4.0	-	-	μs
Data Setup Time	tsDAT		0.2	-	-	μs
Data Hold Time	thDAT		0.2	-	-	μs

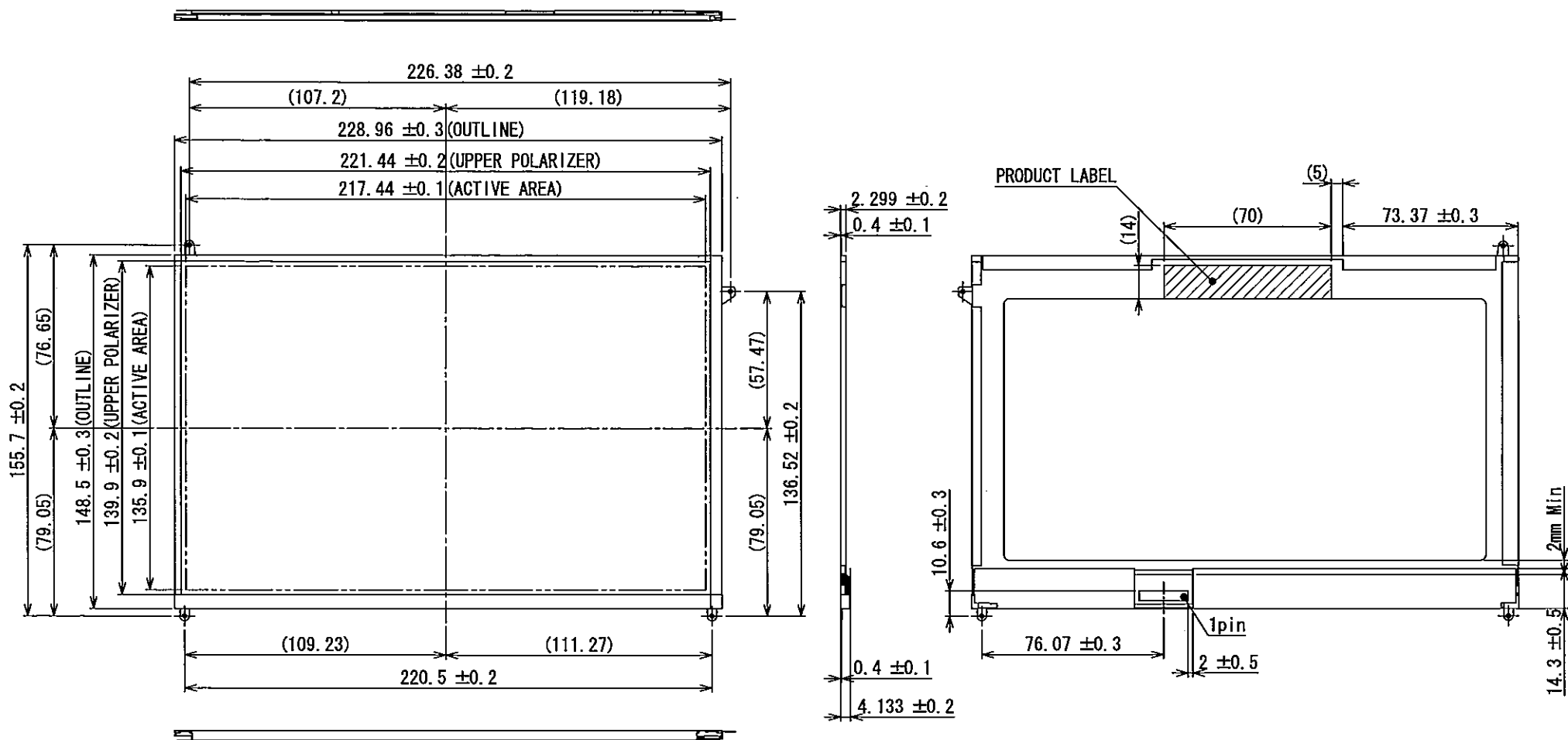
6.4 Timing between interface signals and power supply



SYMBOL	Min.	Typ.	Max.	UNIT	Note
T1	0.3	-	195	ms	
T2	100	-	-	ms	
T3	100	-	-	ms	
T4	35	-	-	ms	
T5	0	-	-	ms	
T6	85	-	-	ms	
T7	0	-	55	ms	
T8	10	-	-	ms	
T10	0	-	-	ms	
T11	0	-	50	ms	

- Note
- 1) When I2C-bus works only in the system side without inputting VBAT, please input IOVDD during bus access.
 - 2) Module side will use I2C bus as a bus master during this period. System side must keep I2C bus high impedance to avoid signal collision.
 - 3) System side can use I2C bus as a bus master during this period.

7. DIMENSIONAL OUTLINE



- Notes 1) The dimension in a parenthesis is a reference value.
2) The general tolerance : $\pm 0.5\text{mm}$

